a first-in-first-out (FIFO) buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter.

23. (New) The apparatus of claim 20 further comprising the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory.

B11 cont'd.

24. (New) The apparatus of claim 20 wherein the apparatus is pipelined.

25. (New) The method of claim 1 further comprising receiving multiple motion compensation commands and performing multiple frame prediction operations in response to the multiple motion compensation commands in a pipelined manner.

REMARKS

Applicants respectfully request reconsideration of the present U.S. Patent application. Claims 1, 6, 11, and 14 have been amended. Claims 17-25 have been added. Therefore, claims 1-25 are pending.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 2, 4, 6, 7, 9, and 11-13 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,652,823 issued to Eto, et al. (*Eto*). For at least the reasons set forth below, Applicants submit that claims 1, 2, 4, 6, 7, 9, and 11-13 are not anticipated by *Eto*.

Claim 1 as amended recites:

> receiving a motion compensation command having associated correction data **related to a macroblock**;
>
> storing the correction data related to a macroblock in a memory according to a first order corresponding to the motion compensation command;
>
> . . .
>
> reading the correction data related to a macroblock from the memory according to a second order; and
>
> . . . .

Thus, Applicants claim a method of receiving, storing in a first order, and reading in a second order correction data related to a macroblock. Claim 6 as amended similarly recites receiving, storing in a first order, and reading in a second order correction data related to a macroblock.

Eto teaches reordering picture **frames** and **groups of pictures** between storing and displaying, a technique well known in the art. See column 34, lines 22 - 33; column 35, lines 13 - 30. *Eto* does not, however, disclose storing correction data related to a **macroblock** in a first order and reading data related to a macroblock in a second order. Therefore, *Eto* does not anticipate the invention as claimed in claims 1 and 6.

Claims 2 and 4 depend from claim 1. Claims 7 and 9 depend from claim 6. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 2, 4, 7, and 9 are not anticipated by *Eto* for at least the reasons set forth above.

Claim 11 as amended recites:

> a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data **related to a macroblock** in a first order determined by the write address generator;
>
> . . .
>
> a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order.

Thus, Applicants claim a circuit to store in a first order and to output in a second order pixel data related to a macroblock.

As discussed above, *Eto* teaches reordering picture **frames** and **groups of pictures** between storing and displaying. *Eto* does not disclose a circuit to store data related to a **macroblock** in a first order and to output the data related to a macroblock in a second order. Therefore, *Eto* does not anticipate the invention as claimed in claim 11.

Claims 12 and 13 depend from claim 11. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 12 and 13 are not anticipated by *Eto* for at least the reasons set forth above.

Claim Rejections - 35 U.S.C. § 103

Claims 3, 5, 8, 10, 15, and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto* as applied to claims 1, 2, 4, 6, 7, 9, and 11-13 in the Office Action, and further in view of *Mizobata* of record (U.S. Patent No. 5,892,518, issued to Mizobata, et al.). For at least the reasons set forth below, Applicants submit that claims 3, 5, 8, 10, 15, and 16 are not unpatentable over *Eto* in view of *Mizobata*.

As set forth above, Applicants claim a method of receiving, storing in a first order, and reading in a second order correction data related to a macroblock in claim 1. Claim 6 similarly recites receiving, storing in a first order, and reading in a second order correction data related to a macroblock. As discussed above, *Eto* does not disclose storing data related to a macroblock in a first order and reading data related to a macroblock in a second order. In claim 11 Applicants claim a circuit to store in a first order and to output in a second order pixel data related to a macroblock. As discussed above, *Eto* does not disclose a circuit to store data related to a macroblock in one order and output data related to a macroblock in a second order.

Mizobata is cited in the Office Action as teaching generation of a bounding box, performing texture operations, and processing circuitry for manipulation of the pixels. Whether or not *Mizobata* teaches the elements set forth in the Office Action, *Mizobata* does not cure the deficiencies of *Eto*. Therefore, no combination of *Eto* and *Mizobata* teaches or suggests storing data related to a macroblock in a first order and reading data related to a macroblock in a second order according to claims 1 and 6, or a circuit to store data related to a macroblock in one order and output data related to a macroblock in a second order according to claim 11. Claims 3 and 5 depend from claim 1. Claims 8 and 10 depend from claim 6. Claims 15 and 16 depend from claim 11. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that the present invention as claimed in claims 3, 5, 8, 10, 15, and 16 is not rendered obvious by the teachings of *Eto* taken together with the teachings of *Mizobata*.

Allowable Subject Matter

Claim 14 was objected to as depending on a rejected base claim, but would otherwise be allowable if rewritten in independent form including the limitations of the base and intervening claims. Claim 14 has been amended as suggested in the Office Action to be in independent for and to include the limitations of the base claim. Therefore, the Applicants submit that claim 14 is in condition for allowance.

Conclusion

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 1-25 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Date: July 12, 2001

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July 12, 2001
Date of Deposit

Deborah L. Higham
Name of Person Mailing Correspondence

Signature 7/12/01 *Date*

AMENDMENTS TO THE CLAIMS WITH MARKINGS

IN THE SPECIFICATION

Please replace the paragraph beginning on page 9, line 13 with:

In general, motion compensation consists of [reconstruction] reconstructing a picture by predicting, either forward, backward, or bi-directionally, the resulting pixel colors from one or more reference pictures. Figure 4 illustrates two reference pictures and a bi-directionally predicted reconstructed picture. In one embodiment, the pictures are divided into 16 pixel by 16 pixel macroblocks; however, other macroblock sizes (e.g., 16x8, 8x8) can also be used. A macroblock is further divided into 8 pixel by 8 pixel blocks.

Please replace the paragraph beginning on page 10, line 5 with:

Figure 5 illustrates a conceptual representation of pixel data suitable for use with the invention. Each macroblock has 256 bytes of luminance (Y) data for the 256 pixels of the macroblock. The blue [chromanance] chrominance (Cb) (U) and red [chromanance] chrominance (Cr) (V) data for the pixels of the macroblock are communicated at 1/4 resolution, or 64 bytes of U data and 64 bytes of V data for the macroblock and filtering is used to blend pixel colors. Other pixel encoding schemes can also be used.

Please replace the paragraph beginning on page 12, line 18 with:

In one embodiment, the [bonding] bounding box is defined by the upper left and lower right corners of the bounding box. The upper left of the bounding box is the origin of the macroblock included in the GFXBLOCK command. The lower right corner of the bounding box is [computer] computed by adding the region height and width to the origin.

Please replace the paragraph beginning on page 12, line 22 with:

In one embodiment, the [bonding] bounding box computes a texture address offset, P_0, which is determined according to:

$$P_{0u} = Origin_x + MV_x \qquad \text{(Equation 1)}$$

and

$$P_{0v} = Origin_y + MV_y \qquad \text{(Equation 2)}$$

where P_{0v} and P_{0u} are offsets for v and u co-ordinates, respectively. $Origin_x$ and $Origin_y$ are the x and y co-ordinates of the bounding box origin, respectively, and MV_x and MV_y are the x and y components of the motion

vector, respectively. The P_0 term translates the texture addresses in a linear fashion.

Please replace the paragraph beginning on page 14, line 4 with:

Mapping address generator 615 provides read addresses to fetch unit 620. The read address generated by mapping address generator 615 and provided to fetch unit 620 are based on pixel movement between frames as described by the motion vector. This allows pixels stored in memory to be reused for a subsequent frame by rearranging the addresses of the pixels fetched. In one embodiment, the addresses generated by mapping address generator 615 using the values listed [abvoe] above simplify to:

$$v(x,y) = y + P_{0v} \qquad \text{(Equation 5)}$$

and

$$u(x,y) = x + P_{0u} \qquad \text{(Equation 6)}$$

Please replace the paragraph beginning on page 16, line 10 with:

The pixels read from texture palette 650 are input to blend unit 670. Blend unit 670 combines the pixel data from bilinear filter 625 with correction data from texture palette 650 to generate an output pixel for a new video frame. Mapping address generator 615 provides fractional pixel positioning information to bilinear filter 625.

Please replace the paragraph beginning on page 16, line 14 with:

Multiple GFXBLOCK commands can exist in the pipeline of Figure 6 simultaneously. As a result correction data [steams] streams through texture palette 650. Read and write accesses to texture palette 650 are managed such that the correction data [steams] streams do not overwrite valid data stored in the texture palette 650.

IN THE CLAIMS

1. (Amended) A method of motion compensation of digital video data, the method comprising:

receiving a motion compensation command having associated correction data related to a macroblock;

storing the correction data related to a macroblock in a memory according to a first order corresponding to the motion compensation command;

performing frame prediction operations in response to the motion compensation command;

reading the correction data related to a macroblock from the memory according to a second order; and

combining the correction data related to a macroblock with results from the frame prediction operations to generate an output video frame.

6. (Amended) An apparatus for motion compensation of digital video data, the apparatus comprising:

means for receiving a motion compensation command having associated correction data related to a macroblock;

means for storing the correction data related to a macroblock in a memory according to a first order corresponding to the motion compensation command;

means for performing frame prediction operations in response to the motion compensation command;

means for reading the correction data related to a macroblock from the memory according to a second order; and

means for combining the correction data related to a macroblock with results from the frame prediction operation to generate an output video frame.

11. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data related to a macroblock in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order.

14. (Amended) [The] A circuit [of claim 11 wherein the second order is] for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block row major order.

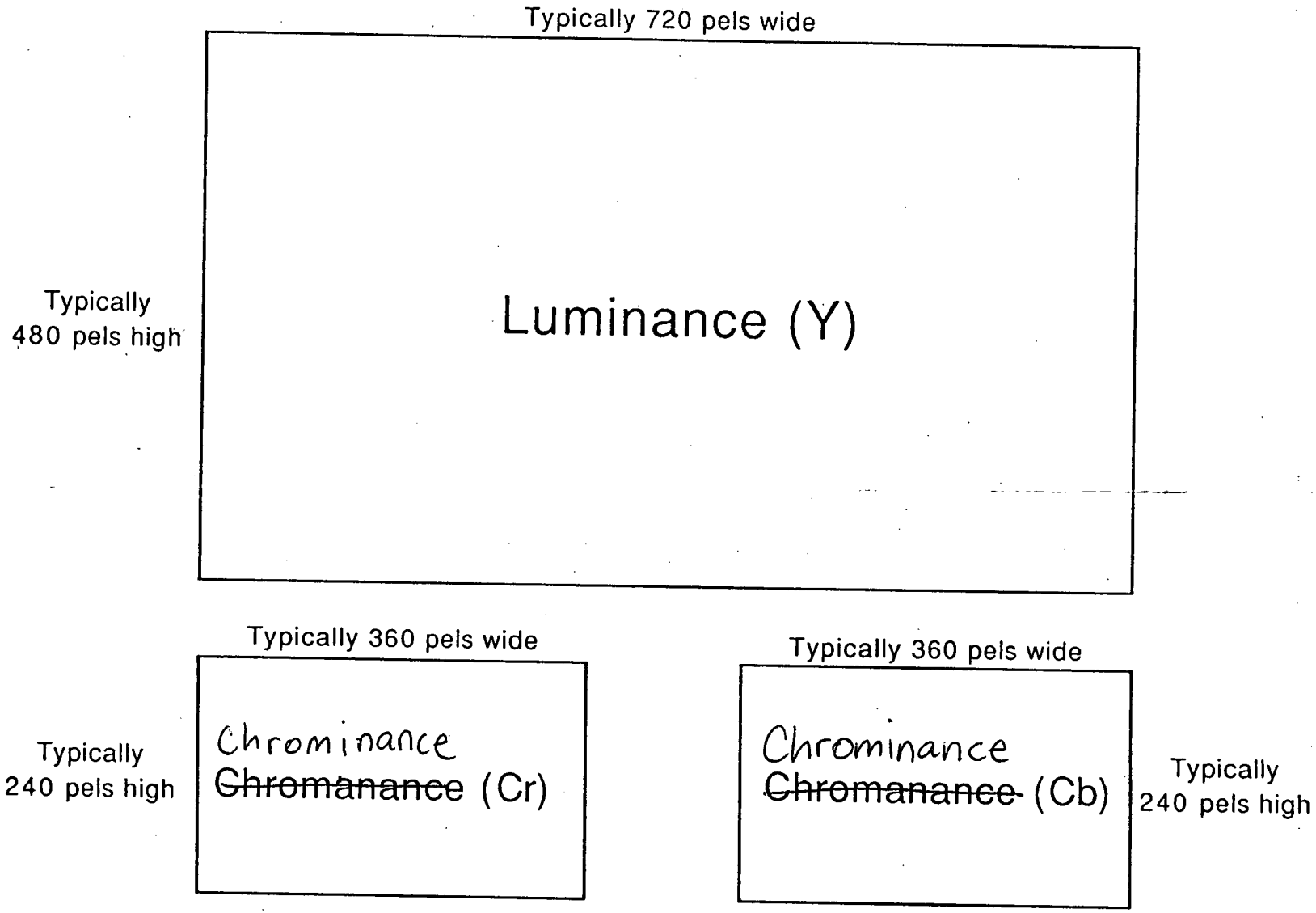
Typically 720 pels wide
Typically
480 pels high
Luminance (Y)
Typically 360 pels wide
Typically
240 pels high
Chrominance
Chromanance (Cr)
Typically 360 pels wide
Chrominance
Chromanance (Cb)
Typically
240 pels high

FIG. 5